

Sheet 1 of 1

FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
		SON-2230	09/964,540
		APPLICANT	
		OKUDA	
LIST OF REFERENCES CITED BY APPLICANT  (Use several sheets if necessary)		FILING DATE	GROUP
		09/28/01	2858

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
PK	AA	5,914,615	06/99	Chess			
	AB						
	AC						
	AD						

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION		
							YES	NO	ABST.
	AE								
	AF								
	AG								

## OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

PK	AH	M.C. Johnson, D. Somasekhar, and K. Roy, "Models and Algorithms for Bounds on Leakage in CMOS Circuits", IEEE Tran. CAD IC Sys., vol. 18, no. 6, pp. 714-725, June 1999.
PK	AI	A. Ferre and J. Figueras, "On Estimating Bounds of the Quiescent Power Supply Current for IDDQ Testing", VLSI Test Sym., pp. 106-111, IEEE, 1996.
PK	AJ	P.C. Maxwell and J.R. Rearick, "Estimation of Defect-Free IDDQ in Submicron Circuits Using Switch Level Simulation", Int. Test Conf., pp. 882-889, IEEE, 1998.
PK	AK	A. Gattiker and W. Mary, "Current Signatures", VLSI Test Sym., pp. 112-117, IEEE, 1996.
PK	AL	C. Thibeault, "On the Comparison of IDDQ and IDDQ Testing", VLSI Test Sym., pp. 143-150, IEEE, 1999.
	AM	
	AN	
	AO	
	AP	

EXAMINER

DATE CONSIDERED



9/12/03

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

DC084736.DOC